

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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Applicants: Se Jeong Park et al. Docket No.: 00-415
Serial No.: Examiner :
Filed : Art Unit :
For : CACHE MEMORY FOR TEXTURE MAPPING PROCESS IN THREE
-DIMENSIONAL GRAPHICS AND METHOD FOR REDUCING
PENALTY DUE TO CACHE MISS

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INFORMATION DISCLOSURE STATEMENT

Hon. Commissioner of Patents & Trademarks
United States Patent & Trademark Office
Washington, D.C. 20231

Dear Sir:

In accordance with the requirements of 37 CFR 1.97 and
1.98, Applicants hereby submit the prior art, copies enclosed.

- (1) An article entitled, "THE CLIPMAP: A VIRTUAL MIPMAP",
By Tanner et al., published by Silicon Graphics
Computer Systems. This article discloses the clipmap,
a dynamic texture representation that efficiently
caches texture of arbitrarily large size in a finite
amount of physical memory for rendering at real-time
rates. The system further describes a software system
for managing clipmaps that supports integration into

demanding real-time applications. We show the scale and robustness of this integrated hardware/software architecture by reviewing an application virtualizing a 170 gigabyte texture at 60 Hertz. Finally, ways are suggested that other rendering systems may exploit the concepts underlying clipmaps to solve related problems.

- (2) An article, entitled "TEXRAM: A SMART MEMORY FOR TEXTURING", By Schilling et al., published May 1996, University of Tübingen. This article discloses integrating arithmetic units and large memory arrays on the same chip and thus exploring the enormous internal transfer rates provides an elegant solution to the memory access bottleneck of high-quality texture mapping. This technology only achieves higher texturing speed at lower system costs, can also incorporate new functionalities such as detail mapping and footprint assembly to produce higher quality-images at real-time rendering speeds. Environment and video mapping are also integrated on the Texram, which therefor represents an autonomous and versatile texturing coprocessor. Logic-enhanced memories might become the computing paradigm of the future, not just

in graphics applications. Technological advances will foster this trend by providing an ever increasing amount of memory capacity and chip space for arithmetic units. As the ultimate solution, a complete 3D graphics pipeline including all memory systems integrated on a single chip.

- (3) An article entitled, "THE DESIGN AND ANALYSIS OF A CACHE ARCHITECTURE FOR TEXTURE MAPPING", By Hakura et al., Computer Systems Laboratory, Stanford University. This article discloses the effectiveness of texture mapping in enhancing the realism of computer generated imagery has made support for real-time texture mapping a critical part of graphics pipelines. Despite a recent surge in interest in three-dimensional graphics from computer architects, high-quality high-speed texture mapping has so far been confined to costly hardware systems that use brute-force techniques to achieve high performance. One obstacle faced by designers of texture mapping systems is the requirement of extremely high bandwidth to texture memory. High bandwidth is necessary since there are typically tens to hundreds of millions of accesses to texture memory per second. In addition, to achieve


the high clock rates required in graphics pipelines,
low-latency access to texture memory is needed. This
paper proposes the use of texture image caches to
alleviate the above bottlenecks, and evaluate various
tradeoffs that arise in such designs.

The undersigned submits the above-identified references for
independent consideration by the Examiner and does not make any
admission that these references are or are not material to the
present invention or that these references are or are not prior
art with respect to the present invention.

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deposited with the United States Postal Service as
Express Mail in an envelope addressed to: Commissioner
of Patents and Trademarks, Washington, D.C. 20231
on June 19, 2000
(Date of Deposit)
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Respectfully submitted,

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